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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,828	03/15/2004	Chien-Ting Lai		3134

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EXAMINER	
DOAN, THERESA T	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 08/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/801,828	LAI ET AL.	
	Examiner	Art Unit	
	Theresa T. Doan	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-11,21,22,24,26 and 28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-11, 21-22, 24, 26 and 28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The Amendment filed on 05/30/06 has being acknowledged. By this amendment, claims 1-2, 4-11, 21-22, 24, 26 and new claim 28 are pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 21 and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee (U.S. Pat. 6,452,210).

Regarding claim 21, Lee (Fig. 3C) discloses a single-gated thin film transistor used in a liquid crystal display device, comprising:

a homogeneous base substrate 30 defining a cavity 30A in an upper face thereof;

a gate electrode 32 being made of metallic material such as Al, Mo, Cr, Ta and an Al alloy (column 3, lines 31-33) and filled in the cavity; a gate insulation layer 34 (column 3, lines 35-37) applied upon the homogeneous base substrate 30 covering both the homogeneous base substrate 30 and gate electrode 32;

a channel layer 36 applied upon the gate insulation layer 34 and only covering a central portion of an upper face of the gate insulation layer 34 ;

a source electrode 40 disposed upon one side of the channel layer 36 and further covering a portion of the gate insulation layer 34 wherein the portion is exposed to an exterior before the source/drain electrode 40 is applied thereto; and

a drain electrode 40 disposed upon the other side of the channel layer 36 and further covering another portion of the gate insulation layer 34 wherein the another portion is exposed to the exterior before the drain electrode 40 is applied thereto (see Fig. 3C and column 3, lines 34-40).

Regarding claim 26, Lee discloses the thin film transistor functioning as a switching device (column 1, lines 20-27), the gate electrode 32 would control the thin film transistor to switch on or off.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-2, 4-5, 7-11, 21-22, 24, 26 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiramatsu et al. (U.S. Pat. 5,311,040) in view of Lee (U.S. Pat. 6,452,210).

Regarding claims 1, 4, 7, 11, 21 and 28, Hiramatsu (Fig. 6E) discloses a single-gated thin film transistor used in a liquid crystal display device (column 1, lines 20-24),

comprising: a transparent homogeneous base substrate 1 made of glass (column 3, lines 25-28); a gate electrode 2 made of Ta metallic material (column 3, lines 25-26); the gate electrode 2 being disposed on the transparent homogeneous base substrate 1; a gate insulation layer (3,4) disposed on the transparent homogeneous base substrate 1 and gate electrode 2; a channel layer disposed on the gate insulation layer (3,4) (column 2, lines 16-18); a source ohmic contact layer and a drain ohmic contact layer 8 (column 3, lines 46-51) arranged on opposite ends of the channel layer; a source electrode 9 (column 4, line 27) disposed on source ohmic contact layer 8, on a portion of the gate insulation layer (3,4), and on the transparent homogeneous base substrate 1, wherein the portion of the gate insulation layer (3,4) is exposed to an exterior (see Fig. 6B) before the source electrode 9 is applied thereto; and a drain electrode 10 (column 4, line 28) disposed on drain ohmic contact layer 8, on a portion of the gate insulation layer (3,4), and on the transparent homogeneous base substrate 1, wherein the portion of the gate insulation layer (3,4) is exposed to an exterior (see Fig. 6B) before the drain electrode 10 is applied thereto.

Hiramatsu does not disclose that the gate electrode 2 is disposed in the transparent base substrate 1.

However, Lee teaches a conventional thin film transistor having a gate electrode 10 being disposed on the substrate 8 (see Fig. 1). Lee further teaches that the conventional thin film transistor shown in Fig. 1 is modified by disposing the gate electrode 32 in the substrate 30 (see Fig. 2) to compensate for step coverage in the thin film transistor (column 2, lines 9-12). Accordingly, it would have been obvious to one

having ordinary skill in the art at the time of the invention was made to modify the thin film transistor of Hiramatsu by disposing the gate electrode 2 in the transparent base substrate 1 because such modification would eliminate step coverage in the gate electrode and would provide a wide selection for a material of the gate electrode, as taught by Lee (column 4, lines 10-18).

Regarding claims 2, 5 and 8, Hiramatsu (Fig. 6E) further discloses that the surface of the gate electrode 2 is parallel with the surface of the transparent homogenous base substrate 1, a cross-section of the gate electrode 2 is trapezoidal, and the gate insulation layer (3,4) is made of silicon nitride or silicon oxide (column 3, lines 31-32).

Regarding claims 9-10, Hiramatsu (Fig. 6E) further discloses that the active layer 5 including the channel layer is made of amorphous silicon (column 5, lines 34-35), and the source and drain ohmic contact layers 8, which are formed by n doped amorphous silicon layer (column 5, lines 39-40).

Regarding claims 22, 24 and 26, Hiramatsu also discloses that the thin film transistor functions as a switching element, the gate electrode controls the thin film transistor to switch on or off (column 1, lines 20-27).

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hiramatsu et al. (U.S. Pat. 5,311,040) in view of Lee (U.S. Pat. 6,452,210) as applied claim 1 above and further in view of Applicant's Admitted Prior Art (AAPA).

Neither Hiramatsu nor Lee discloses that the cross-section of the gate electrode is rectangular.

However, AAPA (Fig. 14) teaches a conventional thin film transistor having the gate electrode 20 being a rectangular shape. Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to change the shape of the gate electrode of Hiramatsu from trapezoid to rectangular because the shape of the gate electrode is not critical. It appears that these changes produce no functional differences and therefore would have been obvious. *In re Woodruff, 919 F. 2d 1575, 1578, 16 USPQ 2d 1934, 1936 (Fed. Cir. 1990).*

Response to Arguments

7. In response to Applicant's arguments with respect to amended claims 1-2, 4-11, 22, 24 and 28, the new reference is applied in the new ground of rejection.

8. With respect to amended claims 21 and 26, Applicant argues that Lee's Fig. 2 does not teach "a homogeneous substrate" as amended.

This argument is not persuasive because it should be noted that it has long been held that the use of the term "comprising" leaves a claim open for inclusion of materials or steps other than those recited in the claims. *Ex parte Davis, 80 USPQ 448 (PTO Bd.*

App. 1948). Use of the term "comprising" does not exclude the presence of other elements. *In re Hunter, 288 F.2d 930, 129 USPQ 25 (CCPA 1961).* Therefore, Lee's Fig. 2 clearly teaches "a homogeneous base substrate" defining a cavity as claimed because the substrate 30 is homogeneous.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Theresa T. Doan whose telephone number is (571) 272-1704. The examiner can normally be reached on Monday to Friday from 7:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, WAEL FAHMY can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Theresa Doan
July 26, 2006.